

## CLAIMS

What is claimed is:

1 Sub B1 1. A method of motion compensation of digital video data, the method  
2 comprising:  
3 receiving a motion compensation command having associated correction data  
4 related to a macroblock;  
5 storing the correction data in a memory according to a first order corresponding to  
6 the motion compensation command;  
7 performing frame prediction operations in response to the motion compensation  
8 command;  
9 reading the correction data from the memory according to a second order; and  
10 combining the correction data with results from the frame prediction operations to  
11 ~~generate an output video frame.~~

1 Sub A3 2. The method of claim 1 the first order is based on output from an Inverse  
2 Discrete Cosine Transform (IDCT) operation.

1 3. The method of claim 1 performing frame prediction operations further  
2 comprises:  
3 generating a bounding box containing the macroblock; and  
4 iterating the bounding box;  
5 fetching reference pixels;

6 filtering the reference pixels;  
7 averaging the filtered reference pixels, if necessary; and  
8 adding correction data to the reference pixels.

1 4. The method of claim 1 wherein the motion compensation data includes at  
2 least one motion vector.

5. The method of claim 1 further comprising performing texturing operations  
for the macroblock.

Sub 68 6. An apparatus for motion compensation of digital video data, the apparatus  
2 comprising:  
3 means for receiving a motion compensation command having associated  
4 correction data related to a macroblock;  
5 means for storing the correction data in a memory according to a first order  
6 corresponding to the motion compensation command;  
7 means for performing frame prediction operations in response to the motion  
8 compensation command;  
9 means for reading the correction data from the memory according to a second  
10 order; and  
11 means for combining the correction data with results from the frame prediction  
12 operations to generate an output video frame.

SUBA7

1 7. The apparatus of claim 6 the first order is based on output from an Inverse  
2 Discrete Cosine Transform (IDCT) operation.

1 8. The apparatus of claim 6 performing frame prediction operations further  
2 comprises:

3 means for generating a bounding box containing the macroblock; and

4 means for iterating the bounding box;

5 means for fetching reference pixels;

6 means for filtering the reference pixels;

7 means for averaging the filtered reference pixels, if necessary; and

8 means for adding correction data to the reference pixels.

1 9. The apparatus of claim 6 wherein the motion compensation data includes  
2 at least one motion vector.

1 10. The apparatus of claim 6 further comprising means for performing  
2 texturing operations for the macroblock.

SUBA5

1 11. A circuit for generating motion compensated video, the circuit comprising:  
2 a command stream controller coupled to receive an instruction to manipulate  
3 motion compensated video data;  
4 a write address generator coupled to the command stream controller;

0922474-010799

5 a memory coupled to the command stream controller and to the write address  
6 generator, the texture palette to store pixel data in a first order determined by the write  
7 address generator;  
8 processing circuitry coupled to the write address generator to receive control  
9 information and data from the command stream controller to generate a reconstructed  
10 video frame;  
11 a read address generator coupled to the processing circuitry and to the memory,  
12 the read address generator to cause the memory to output pixel data in a second order.

1 12. The circuit of claim 11 wherein the first order is block-by-block row major  
2 order.

1 Sub D1 13. The circuit of claim 11 wherein the first order corresponds to an output  
2 sequence of an inverse discrete cosine transform operation.

1 Sub B10 14. The circuit of claim 11 wherein the second order is sub-block-by-sub-  
2 block row major order.

1 Sub D2 15. The circuit of claim 11 wherein the processing circuitry comprises a setup  
2 engine that determines a bounding box for pixels manipulated by the instruction, wherein  
3 the bounding box contains all edges of a macroblock.

1 16. The circuit of claim 11 wherein the processing circuitry comprises a  
2 windower having a first mode wherein pixels inside a triangle within a bounding box are  
3 processed, and a second mode wherein all pixels within the bounding box are processed.

ADD B<sup>11</sup>



05227174-010799